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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,705	02/19/2004	Myoung-Bo Kwak	8021-193 (SS-18611-US)	5552

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EXAMINER	
MATIN, NURUL M	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,705	KWAK, MYOUNG-BO	
	Examiner	Art Unit	
	Nurul M. Matin	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,13,14,16,19 and 20* is/are rejected.

7)☒ Claim(s) *9,11,12,15,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/29/2007 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 16 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5, 10, 16, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted Prior Art (fig.1) [hereinafter, refer to as "Prior Art"] in view of Nakamura, US 2002/0154723 and further in view of Shirota et al, US 2003/0142773.

Re claim 1, Prior art teaches a data recovery apparatus for recovering effective data from serial data received via a high-speed serial link (fig.1, page 1, Para [0017]), the data recovery apparatus comprising: a clock signal generating circuit that generates at least two clock signal groups, comprising first and second clock signal groups (fi.q.1, page 1, Para [0017], where PLL (11) is a clock signal generating circuit and it generates three clock signal groups (CLKA, CLKB, CLKC).), and a data recovery circuit that recovers the effective data from the serial data by oversampling the serial data(fig.1 &2, page 1, Para [0019, "a triple (OSR=3) oversampling circuit is adapted to recover clock signals and data from differential serial data in a band of several giga bits per second"]. But Prior art fails to teach that each of the first and second clock signal groups comprises at least two different inputted clock signals having different phases from each other; and a data recovery circuit that recovers the effective data from the serial data by using a dynamically selected one of the at least two clock signal groups, the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data. However Nakamura does teach each of the first and second clock signal groups comprises at least two different inputted clock signals having different phases from each other(page 7, Para [0088], "The phase locked loop 32 generates differential clock signals CKa and CKb each having a clock frequency of 312.5 MHz. The differential clock signals CKa and CKb have a clock period of 3200 ps and are different in phase from each other"). But Prior art and Nakamura fail to teach a data recovery circuit that recovers the effective data from the serial data by using a dynamically selected one of the at least two clock

signal groups, the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data. However, Shirota does teach a data recovery circuit that recovers the effective data from the serial data by using a dynamically selected one of the at least two clock signal groups, the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data (page 2,para [0035], line 8-10 & page1, Para [0011], line 1-11, "The PLL circuit 103 generates a clock signal group 109 consisting of a plurality of clock signals of 480 MHz with different phases and an edge detector for generating edge position information by using a receiver output as a clock signal, and by comparing phases of a plurality of clock signals constituting a clock signal group with a phase of an edge of the receiver output; a clock selection signal generating circuit for generating, using the receiver output as a clock signal, a clock selection signal in response to the edge position information; a clock selection circuit for selecting a clock signal from the clock signal group in response to the clock selection signal").

Therefore, taking the combined teaching of Prior art, Nakamura and Shirota as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of each of the first and second clock signal groups comprises at least two different clock signals having different phases from each other as thought in Nakamura into Prior art to enable to cope with a further high-speed of data transmission in a field of oversampling clock recovery which meets a high-speed data communication. And also the arrangement of a data recovery circuit that recovers the effective data from the

serial data by using a dynamically selected one of the at least two clock signal groups, the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data as thought in Shirota into Prior art and Nakamura for the benefit of recovering very high-rate data.

Re claim 2, Prior art, Nakamura and Shirota references teach the data recovery apparatus of claim 1, and Shirota reference teaches a clock signal selecting circuit that selects one of the at least two clock signal groups in response to a clock selection signal (page 1, Para [0011], 1-11); and Prior art reference also teaches an oversampler that latches the serial data in response to the selected one of the at least two clock signal groups to output OSR bits of sampling data per each bit of serial data; and a clock and data recovery circuit that selects one of the OSR bits of sampling data per each bit of serial data as effective data; and outputs the clock selection signal in response to logic values of the bits of sampling data(page 1, Para[0017], line 6-14).

Re claim 3, Prior art, Nakamura and Shirota references teach the data recovery apparatus of claim 2, and Prior art references also teaches the clock signal generating circuit comprises: a phase-locked loop that generates at least OSR sampling clock signals each having different phases (page 1, Para [0017], line 6-7).

Re claim 5, prior art, Nakamura and Shirota references teach the data recovery apparatus of claim 1, and prior art reference also teaches the first clock signal group comprises OSR sampling clock signals having OSR different phases, wherein OSR is at least 3 and the second clock signal group comprises OSR clock signals having multiple

phases that are all different from the OSR phases of the first clock signal group (page 1, Para [0017], line 6-8).

Re claim 10, Prior art and Shirota references teach the data recovery apparatus of claim 5, and Shirota reference also teaches the clock signal selecting circuit comprises a plurality of multiplexers that receive the first and second clock signal groups and output one of the first and second clock signal groups in response to the clock selection signal (see fig.2, it shows that two input goes into the selection signal and generating one output).

Re claim 16 and 19, which claims the same subject matter as recited in claim 1. Therefore, claims 16 and 19 have been analyzed and rejected with respect to claim 1.

Re claim 20, Prior art teaches a data recovery method for recovering effective data from an input stream of serial data having an eye open region and a plurality of zero-crossing transitions, the method comprising: oversampling each bit of the serial data at an oversampling rate of OSR, and latching OSR bits of sampling-data for each bit of serial data according to a selected one set of OSR sampling clock signals selected from among a first and second set of OSR sampling clock signals (page1, Para [0017], line 10-18, Para [0019]. But prior art fail to teach that each set of OSR sampling clock signals comprise at least two different inputted clock signals having different phases from each other; and wherein the selected set of OSR sampling clock signals has been dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data. However, Nakamura does teach each set of OSR sampling clock signals comprise at least two different

inputted clock signals having different phases from each other (page 7, Para [0088], "The phase locked loop 32 generates differential clock signals CKa and CKb each having a clock frequency of 312.5 MHz. The differential clock signals CKa and CKb have a clock period of 3200 ps and are different in phase from each other"). But Prior art and Nakamura fail to teach the selected set of OSR sampling clock signals has been dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data. However, Shirota does teach the selected set of OSR sampling clock signals has been dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data (page 2,para [0035], line 8-10 & page1, Para [0011], line 1-11, "The PLL circuit 103 generates a clock signal group 109 consisting of a plurality of clock signals of 480 MHz with different phases and an edge detector for generating edge position information by using a receiver output as a clock signal, and by comparing phases of a plurality of clock signals constituting a clock signal group with a phase of an edge of the receiver output; a clock selection signal generating circuit for generating, using the receiver output as a clock signal, a clock selection signal in response to the edge position information; a clock selection circuit for selecting a clock signal from the clock signal group in response to the clock selection signal").

Therefore, taking the combined teaching of Prior art, Nakamura and Shirota as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of each set of OSR sampling clock signals comprise at least two different inputted clock signals having different phases from each other as thought in Nakamura

into Prior art to enable to cope with a further high-speed of data transmission in a field of oversampling clock recovery which meets a high-speed data communication. And also the arrangement of the selected set of OSR sampling clock signals has been dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data as thought in Shirota into Prior art and Nakamura for the benefit of recovering very high-rate data.

5. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (figs.I&2) [hereinafter, refers to as "prior art"], Nakamura, US 2002/0154723, Shirota et al, US 2003/0142773 and in view of Sato et al, US 6807233.

Re claim 4, Prior art, Nakamura and Shirota references discloses the data recovery apparatus of claim 2, and Prior art references also discloses the clock signal generating circuit comprises: a phase-locked loop that generates the first group of OSR clock signals (page 1, Para [0017], line 6-7). But they fail to disclose a sub-clock signal generating circuit that generates the second group of OSR clock signals. However, Sato does teach a sub-clock signal generating circuit that generates the second group of OSR clock signals (col.4, line 22-24).

Therefore, taking the combined teaching of Prior art, Nakamura, Shirota and sato as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of a sub-clock signal generating circuit that generates the second group of OSR clock signals as thought in Sato into Prior art, Nakamura and Shirota so

that it is possible to transmit en bloc signals by different sampling frequencies as well as to easily reconstruct and restore these sample data.

Re claim 6, Prior art, Nakamura and Shirota references teach the data recovery apparatus of claim 5, and Prior art reference teaches the phase-locked loop generates first, second, and third sampling clock signals such that rising edges of the first, second, and third sampling clock signals are arranged at equal intervals. But they fail to disclose the sub-clock signal generating circuit generates fourth, fifth, and sixth sampling clock signals so that rising edges of the forth, fifth, and sixth sampling clock signals are arranged at equal intervals. However, Sato does (col.4, line 22-24, It would have been obvious to one of ordinary skill in the art to use first clock in place of second clock, therefore having two clocks with each clock has three outputs).

Therefore, taking the combined teaching of Prior art, Nakamura, Shirota and Sato as a whole,, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of a sub-clock signal generating circuit that generates the second group of OSR clock signals as thought in Sato into Prior art, Nakamura and Shirota so that it is possible to transmit en bloc signals by different sampling frequencies as well as to easily

reconstruct and restore these sample data.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (figs.I&2) [hereinafter, refers to as "prior art"], Nakamura, US 2002/0154723, Shirota et al, US 2003/0142773 and in view of Baba et al, US 5528198.

Re claim 7, Prior art, Nakamura and Shirota fail to teach a first sub-clock signal generating circuit that generates the fourth sampling clock signal in response to the first and second sampling clock signals; a second sub-clock signal generating circuit that generates the fifth sampling clock signal in response to the second and third sampling clock signals; and a third sub-clock signal generating circuit that generates the sixth sampling clock signal in response to the first and third sampling clock signals. However, Baba does (col.8, line 60-co1.9, line 2, the third clock signal 16 is input to the first unit selection circuit 66 as the sub clock. The fourth clock signal 17 is input to the second unit selection circuit 67 as the sub clock. In the same manner, the first clock signal 14 and the second clock signal 15 are input to the third unit selection circuit 68 and the fourth unit selection circuit 69 respectively as the sub clocks).

Therefore, taking the combined teaching of Prior art, Nakamura, Shirota and Baba as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of a first sub-clock signal generating circuit that generates the fourth sampling clock signal in response to the first and second sampling clock signals; a second sub-clock signal generating circuit that generates the fifth sampling clock signal in response to the second and third sampling clock signals; and a third sub-clock signal generating circuit that generates the sixth sampling clock signal in response to the first and third sampling clock signals as thought in Baba into Prior art and Shirota to preset the oscillation frequency to the frequency of the data signal to the input).

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (figs.I&2) [hereinafter, refers to as "prior art"], Nakamura, US 2002/0154723, Shirota et al, US 2003/0142773, Baba et al, US 5528198 in view of Boss, US 7103343.

Re claim 8, Prior art, Nakamura, Shirota and Baba fail to teach the first, second, and third sub-clock signal generating circuits are interpolators. However, Boss does (col.2, line 57-58,' the first interpolator is provided in order to convert the converter clock).

Therefore, taking the combined teaching of Prior art, Nakamura, Shirota, Baba and Boss as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the first, second, and third sub-clock signal generating circuits are interpolators as thought in Boss into Prior art and Shirota to derived from the reference clock into a desired clock for further digital processing of the data.

Allowable Subject Matter

8. Claims 9, 11, 12, 15, 17, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nurul M. Matin whose telephone number is 571-270-1188. The examiner can normally be reached on mon-fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nurul Matin
Examiner.

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER